CONFIGURATION IN A CONFIGURABLE SYSTEM ON A CHIP

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BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates generally to a configurable system on a chip (CSoC), and specifically to structures and methods regarding the configuration of the CSoC.

Description of the Related Art

Programmable logic devices, such as field programmable logic devices (FPLDs), are programmed to perform user-specified logic functions by loading configuration data into the FPLD. This configuration data is typically loaded into the FPLD as a bitstream, i.e. a string of binary bits. Each bit programs a specific programmable resource on the device. Thus, some bits configure the logic blocks which perform the user-defined logic functions, other bits configure the input/output blocks which interface to devices external to the FPGA, and yet other bits configure the programmable interconnect that connects the logic blocks and the input/output blocks.

Typically, the configuration data is stored in a nonvolatile memory device and loaded into the FPLD upon device power-up. The configuration information is loaded into the FPLD in data frames using a shift register. This shift register has N serially coupled one-bit shift registers, each register clocked by the same clock signal. As the bitstream is serially shifted into the shift